Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-42. (canceled)

43. (currently amended) A recessed gate field effect power MOS device having a vertically-oriented channel comprising:

a semiconductor substrate including first and second laterally-extending layers of first and second opposite polarity dopants defining a body layer and an underlying drain layer;

a first trench having sidewalls extending depthwise from an upper surface of the substrate at least through the body layer to a bottom wall at a predetermined depth from the upper surface of the substrate;

a gate oxide layer on the trench sidewalls and the bottom wall of the first trench;

a gate conductor disposed over the gate oxide layer within the first trench to a depth of at least an elevation of the upper surface of the substrate;

a vertically-oriented layer of semiconductor material extending upwardly along the gate oxide layer on the side thereof opposite the first trench, the vertically-oriented layer extending from the body layer to the upper surface of the substrate, the vertically-oriented layer comprising a first vertical layer portion contiguous with the body layer doped with said first polarity dopant to define an active body region including a vertical channel, and a second vertical layer portion atop the first vertical layer portion and forming a PN junction therewith, the second vertical layer portion being doped with said second polarity dopant to form a source region contacting the active body region; and

a vertically-extending source conductor contacting the vertically-oriented layer on a side thereof opposite the gate oxide layer and gate conductor, the source conductor electrically shorting the source region to the active body region across the PN junction;

the gate conductor comprising doped polysilicon contacting the gate oxide layer within the trench and a first metal layer defining a gate metal layer ~~coextending over~~ overlying the doped polysilicon of the gate conductor;

an insulating layer overlying the gate conductor; and

an upper metal layer over the insulating layer and having a first portion contacting the gate conductor through a via in the insulating layer and a second portion coupled to the source region in electrical isolation from the gate conductor.

44. (canceled)

45. (canceled)

46. (canceled)

47. (previously presented) A recessed gate field effect power MOS device according to claim 43 in which the first vertical layer portion has a lateral thickness less than a vertical height thereof.

48. (previously presented) A recessed gate field effect power MOS device according to claim 43 in which the first vertical layer portion has a lateral thickness less than 1 μm.

49. (previously presented) A recessed gate field effect power MOS device according to claim 48 in which the first vertical layer portion contiguous with the body layer is doped to a first doping concentration and a laterally-extending portion of the body layer subjacent the first vertical layer portion has at least a top portion doped to a second doping concentration greater than the first doping concentration.

50. (currently amended) A recessed gate field effect power MOS device according to claim 43 including a vertically-oriented sidewall spacer extending upward from the upper surface of the substrate, the vertically-oriented sidewall spacer atop the vertically-oriented ~~layers~~ layer.

51. (previously presented) A recessed gate field effect power MOS device according to claim 50 including first and second ones of said vertically-oriented layer on respective sides of the trench, each of the first and second ones having one of said vertically-oriented sidewall spacer thereon, and an insulative layer extending laterally between the sidewall spacers over the gate conductor.

52. (currently amended) A recessed gate field effect power MOS device according to claim 51 ~~including an~~ in which the upper metal layer ~~extending~~ extends over the insulative layer and the vertically-oriented sidewall spacer and ~~contacting~~ contacts the vertically-extending source conductor.

53. (previously presented) A recessed gate field effect power MOS device according to claim 43 in which the vertically-extending source conductor contacts a laterally-extending portion of the body layer at a position spaced below the PN junction.

54. (previously presented) A recessed gate field effect power MOS device according to claim 53 in which the first vertical layer portion is doped to a first doping concentration defining a threshold voltage of the channel and the laterally-extending body layer is doped to a second doping concentration greater than the first doping concentration.

55. (previously presented) A recessed gate field effect power MOS device according to claim 43 in which the first trench and the gate oxide layer and gate conductor within the trench form a gate structure which is laterally patterned in two dimensions to define an interconnected matrix enclosing a plurality of islands, each of said plurality of islands containing a downward extending finger of source conductor surrounded by a portion of the active body region including said vertical channel, the channel having a width defined in each island by a perimetral length of the island.

56. (previously presented) A recessed gate field effect power MOS device according to claim 43 wherein the first trench, the gate oxide layer and the gate conductor together form a gate structure configured as a finger, said recessed gate field effect power MOS device comprising a plurality of said fingers;

the source conductor intermediate the fingers of said plurality of fingers to define an interdigitated source-gate structure.

57. (previously presented) A recessed gate field effect power MOS device according to claim 43 including at least two of said first trench spaced laterally apart with two of said vertically-oriented layer of semiconductor substrate defining a second trench between the two of said first trench, each first trench containing the gate oxide layer and gate conductor, said source conductor extending into the second trench and contacting the bottom of the second trench and the respective sides of the two vertically-oriented layers.

58. (previously presented) A recessed gate field effect power MOS device according to claim 43 in which the substrate includes a base layer of said first polarity dopant such that the device defines an alternating PNPN four-layer structure wherein the body layer defines a base of an upper bipolar transistor and a collector of a lower bipolar transistor.

59. (previously presented) A recessed gate field effect power MOS device according to claim 43 in which the gate oxide layer includes a first portion having a first thickness in a lower portion of the trench and a second portion having a second thickness in an upper portion of the trench, the first thickness being greater than the second thickness.

60. (previously presented) A recessed gate field effect power MOS device according to claim 43 wherein the gate metal layer comprises aluminum.

61. (previously presented) A recessed gate field effect power MOS device according to claim 43 wherein the gate metal layer comprises a plateable metal.

62. (previously presented) A recessed gate field effect power MOS device according to claim 43 wherein the gate conductor comprises a refractory metal silicide over the doped polysilicon, and beneath the gate metal layer.

63. (previously presented) A recessed gate field effect power MOS device according to claim 62 wherein the gate metal layer comprises a plateable metal.

64. (previously presented) A recessed gate field effect power MOS device according to claim 62 wherein the gate metal layer comprises aluminum.

65. (currently amended) A recessed gate field effect power MOS device according to claim [[44]] 43, wherein the gate metal layer comprises aluminum, and the upper metal layer comprises aluminum.

66. (currently amended) A recessed gate field effect power MOS device according to claim [[44]] 43, wherein the gate metal layer comprises aluminum, and the insulating layer comprises at least one of the group consisting of oxide, nitride, oxy-nitride, glass, and phosphosilicate glass (PSG).

67.-97. (canceled)

98. (currently amended) ~~A~~ An insulated gate power MOSFET device comprising:

a semiconductor substrate, the substrate comprising drain semiconductor material of a first dopant type;

source semiconductor material of a dopant type the same as said first dopant type;

channel semiconductor material of a second dopant type disposed between the source semiconductor material and the drain semiconductor material, the channel semiconductor material operative under field effect to conduct current between the source semiconductor material and the drain semiconductor material;

a conductive gate structure configured to enable provision of a field to the channel semiconductor material;

a gate oxide layer disposed between the conductive gate structure and the channel semiconductor material;

said conductive gate structure comprising a doped ~~a~~ polysilicon layer ~~contacting~~ overlying the gate oxide layer; ~~and~~

a first metal layer ~~disposed substantially coextensively~~ comprising aluminum including a first portion extending over the doped polysilicon and a second portion contacting the source semiconductor material;

an insulating layer disposed over said gate structure and between the first and second portions of the first metal layer; and

a second metallization over said insulating layer, the second metallization having a first portion contacting the first portion of the first metal layer on the gate structure through

said insulating layer and a second portion contacting said second portion of the first metal layer.

99. (currently amended) A power MOSFET device according to claim 98 wherein ~~the metal layer of the conductive gate structure comprises aluminum,~~ the conductive gate structure further ~~comprising~~ comprises a refractory metal-silicide between the doped polysilicon layer and the aluminum.

100. (currently amended) A power MOSFET according to claim 98 wherein the first metal layer ~~of the conductive gate structure~~ comprises plateable metal.

101. (currently amended) A power MOSFET according to claim ~~100~~ 98 wherein the ~~insulative~~ insulating layer is deposited at a temperature less than 430~~C°~~ ° C.

102. (canceled)

103. (currently amended) A power MOSFET according to claim 98 wherein the second metallization ~~over said insulating layer~~ comprises aluminum.

104.-107. (canceled)